What is claimed is:

1. A storage device comprising:

mode circuitry configured to select between a burst mode and a pipelined mode; and

pipelined/burst circuitry coupled to the mode selection circuitry and configured to switch between the pipelined mode and the burst mode for operating the storage device in either mode.

2. The storage device of Claim 1 wherein the burst mode and the pipelined mode are extended data out modes of operation.

3. The storage device of Claim 1 wherein the pipelined mode is an extended data out mode.

4. The storage device of Claim 1 wherein the burst mode is an extended data out mode.

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~~11.~~ A storage device comprising:

control logic for selecting between a patternless addressing scheme and a patterned addressing scheme; and

switching circuitry for switching between a first pathway and a second pathway depending on which of said patternless addressing scheme and said patterned addressing scheme is selected.

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~~12.~~ A storage device, as in Claim ~~11~~, wherein the storage device is asynchronous.

Sub D1

13. A storage device, as in Claim 11, wherein the first pathway and the second pathway are coupled to a temporary storage device for providing at least one external address to the switching means .

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~~14.~~ A storage device, as in Claim ~~13~~, wherein the external address is temporarily stored in the temporary storage device prior to being sent to a decoder.

Sub C

~~15.~~ A storage device, as in Claim 14, further compromising a counter coupled for receiving a selected portion of the external address for generating an internal address.

Sub D2

6 ~~16.~~ A storage device, as in Claim 5 ~~15~~, wherein the internal address is provided to temporary storage device through the switching circuitry.

7 ~~17.~~ A storage device, as in Claim 6 ~~16~~, wherein the patternless addressing scheme provides a pipelined extended data out pattern.

8 ~~18.~~ A storage device, as in Claim 7 ~~17~~, wherein the patterned addressing scheme provides a burst extended data out pattern.

9 ~~19.~~ A storage device, as in Claim 8 ~~18~~, wherein the switching circuitry includes at least one multiplexed device.

Sub D3

20. A storage device, as in Claim 11, wherein the patternless addressing scheme is for random column address access, and the patterned addressing scheme is for sequence column address access.

21. A storage device, as in Claim 20, wherein the sequence column address access is selected from a group consisting of interleaved and linear column address access.

5. The storage device of Claim 1 wherein the pipelined/burst mode circuitry includes a storage device, the storage device for storing an address.

6. The storage device of Claim 5 wherein the pipelined/burst mode circuitry includes at least one counter for incrementing the address.

7. The storage device of Claim 1 wherein the pipelined/burst mode circuitry is coupled for receiving an external address.

8. The memory device of Claim 7 wherein the pipelined/burst mode circuitry includes a storage device for storing the external address.

9. The storage device of Claim 7 wherein the pipelined/burst mode circuitry includes multiplexed devices for providing an internally generated address to the storage device.

10. The storage device of Claim 1 wherein the storage device is an asynchronous memory.

22. A memory circuit comprising:

control logic for providing a selected mode control signal;

selection and temporary storage circuitry for receiving and storing a first external address; and

a multiplexer coupled to the selection and temporary storage circuitry and to the control logic for receiving the first external address and the selected mode control signal respectively therefrom and for switching between a burst mode and a pipelined mode.

23. A memory circuit, as in Claim 22, wherein the control logic receives an external mode select signal for determining the selected mode control signal.

24. A memory circuit, as in Claim 22, wherein the control logic includes mode circuitry for providing the selected mode control signal, the mode circuitry coupled for receiving an enable signal for determining the selected mode control signal.

25. A memory circuit, as in Claim 24, wherein the enable signal is selected from a group consisting of write enable and output enable signals.

26. A memory circuit, as in Claim 22, wherein the selection and temporary storage circuitry is coupled to a counter.

27. A memory circuit, as in Claim 26, wherein the counter is used for incrementing the first external address when in the burst mode.

28. A memory circuit, as in Claim 26, wherein the selection and temporary storage circuitry is coupled for receiving the first external address and a second external address subsequent thereto for operating in the pipelined mode.

29. A memory circuit, as in Claim 28, wherein the pipelined mode and the burst mode are extended data out modes.

30. A memory circuit, as in Claim 29, wherein the pipelined mode and the burst mode have no column address strobe cycle latency during a write cycle.

31. A memory circuit, as in Claim 30, wherein the pipelined mode and the burst mode have at least a two column address strobe cycle latency during a read cycle.

32. A memory circuit, as in Claim 31, further comprising an asynchronously-accessible memory array coupled for receiving the first external address.

33. A method for accessing a storage device, the method comprising steps of:

receiving a first address to the storage device;

selecting between a burst and a pipelined mode of operation of the storage device;

selecting between outputting information from and inputting information to the storage device;

obtaining a second address to the storage device; and

accessing a storage element of the storage device using the first address and the second address;

the storage device being asynchronously-accessible in either of the burst mode and the pipelined mode.

34. A method, as in Claim 33, further comprising a step of switching as between the burst mode and the pipelined mode.

35. A method, as in Claim 33, wherein the second address is an external address.

36. A method for accessing a random access memory comprising steps of:

receiving an external row address to the memory;

selecting between a burst mode and a pipelined mode of operation;

selecting between a read and a write operation; and

obtaining a first external column address for accessing the memory.

37. A method, as in Claim 36, further comprising a step of:

obtaining a second external column address subsequent to the first external column address for operation in the pipelined mode.

38. A method, as in Claim 36, further comprising a step of:

generating an internal column address subsequent to the first external column address for operation in the burst mode, the internal column address being patterned after the first external column address.

39. A method, as in Claim 36, further comprising a step of:

selecting at least one address pathway based on the selection as between the burst mode and the pipelined mode.

40. A memory integrated circuit comprising:

a memory;

a plurality of input/output pins for providing information to and from the memory;

a plurality of address pins for providing addresses to the memory for providing the information to and from the memory; and

a mode select pin for switching as between a burst mode and a pipelined mode of operation of the memory integrated circuit.

41. The memory of Claim 40 wherein the burst mode and the pipelined mode are extended data out modes.

42. The memory of Claim 40 wherein the memory is an asynchronously-accessible dynamic random access memory.

43. A memory module comprising:

a plurality of memories of which at least one of said memories includes a mode select pin for switching as between a burst mode and a pipelined mode of operation.

44. The memory module of Claim 43 wherein each of the plurality of memories include said mode select pin for switching as between the burst mode and the pipelined mode of operation.

45. The memory module of Claim 43 wherein said one of said memories is an asynchronously-accessible dynamic random access memory.

46. Method for accessing several different locations in an asynchronously-accessible memory device, the method comprising steps of:

selecting a first mode of operation;

providing a new external address for every access associated with asynchronously accessing the device while in the first mode of operation;

switching modes to a second mode of operation;

providing an initial external address associated with asynchronously accessing the device in the second mode of operation; and

generating at least one subsequent internal address patterned after the initial external address while in the second mode of operation.

47. The method of Claim 46 wherein the first mode of operation is a pipelined mode, and the second mode of operation is a burst mode.

48. The method of Claim 47 wherein the burst mode operates in an environment selected from the group consisting of column-based switching, row-based switching, application based switching, and fixed access-based switching.

49. The method of Claim 47 wherein the pipelined mode operates in an environment selected from the group consisting of column-based switching, row-based switching, application based switching, and fixed access-based switching.

50. A system comprising:

a microprocessor;

a memory, coupled to the microprocessor, for operating in burst or pipelined modes; and

a system clock coupled to the microprocessor, the memory not operating directly off the system clock.

51. Method for switching between modes of operation, the method comprising steps of:

maintaining a first enabling signal in an active state;

maintaining a mode select signal to select a first mode;

receiving an initial external address;

cycling a second enabling signal from inactive to active and so forth;

generating an internal address on a cycle of the second enabling signal base on the initial external address;

changing the mode select signal to select a second mode while maintaining the first enabling signal in the active state, and

receiving an external address on each cycle of the second enabling signal.

52. The method of Claim 51 wherein the first enabling signal is a row-address-strobe signal, and the second enabling signal is a column-address-strobe signal.

53. The method of Claim 51 wherein the first mode is a burst mode, and the second mode is a non-burst mode.

54. The method of Claim 53 wherein the non-burst mode is a pipelined mode.

55. Method for switching between modes of operation, the method comprising steps of:

maintaining a first enabling signal in an active state;

maintaining a mode select signal to select a first mode;

receiving a stream of addresses and cycling a second enabling signal for processing the stream of addresses; and

changing the mode select signal to select a second mode.

56. The method of Claim 55 further comprising steps of:

receiving an external address; and

generating one or more internal addresses based on the external address while in the second mode.

57. The method of Claim 55 wherein the changing of the mode select signal is accomplished while maintaining the first enabling signal in the active state.

58. The method of Claim 57 wherein the first mode is a pipelined mode, and the second is a burst extended data out mode.